

EE

Evaluation Engineering

OCTOBER 2008

*Written by Engineers...
for Engineers*

IC ATE
**Tackling Next-Generation
RF SOC Test**

**Environmental Test
Applications**

Signal Analyzers
Extended Capabilities
Blur Distinctions

X-Ray Inspection
Exploring AOI and X-Ray

Tackling Next-Generation RF SOC Test

by Ron Burke, Teradyne

Developing an automated production test solution for current and next-generation complex RF SIP/SOC devices is an increasingly difficult task. Both the test program and the device interface board (DIB) that mounts between the ATE system and the device handler are substantially more challenging design efforts for 3/4G devices.

In the past, the typical 2G RF device had four to six RF ports supporting one or more communications standards, such as GSM and EDGE, with two to four operating bands. With increased device integration and consumer demand for more features, the typical number of RF ports on today's RF SIP/SOC has increased to between 16 and 22, supporting multistandard devices and MIMO capability in the new releases of 3.9/4G LTE standards.

Developing an efficient quad-site ATE solution for the next-generation multiple standard WEDGE (combined GSM, EDGE, WCDMA, and LTE) transceiver with 22 RF ports presents a daunting task for test engineers. Despite the increase in complexity and design/development risks, test engineers nonetheless must deliver a solution with a lower overall cost-of-test (COT) on the same time-to-market (TTM) interval as previous devices.

DIB Development

The first problem to tackle is development of the DIB between the ATE system and the DUT. To mitigate test-time and equipment-cost increases, the

DIB must be designed to maximize throughput by testing multiple DUTs at the same time.

The first step is to map the available system resources to the device pin requirements. Given a WEDGE transceiver device, a quad-site solution will require 88 RF ports plus baseband, digital, and DC resources. A WEDGE world transceiver can include one reference clock input port, seven transmit ports, and seven primary and seven diversity receive ports.

The ATE system must be able to source a reference clock signal connected to all four sites in parallel. To test the DUT transmit paths in minimal time, the quad-site DIB must provide 28 paths from the four devices to the ATE measurement instrument, four in parallel simultaneously. To test the receive paths of the DUT, the quad-site DIB must offer 56 source paths from the ATE system to the four sites.

To minimize test time, the ATE system and DIB must support testing of both the primary and diversity receive paths in parallel for all four sites. To test the DUT's primary and diversity receive channels in parallel for quad-site, eight parallel source channels are required.

RF ATE systems from the 2G era lack these necessary RF connections, the instruments were not designed for high port count devices, and the instrument ports typically were designed for optimized tasks. Some 2G RF ATE instruments were designed with symmetrical port configurations; however,

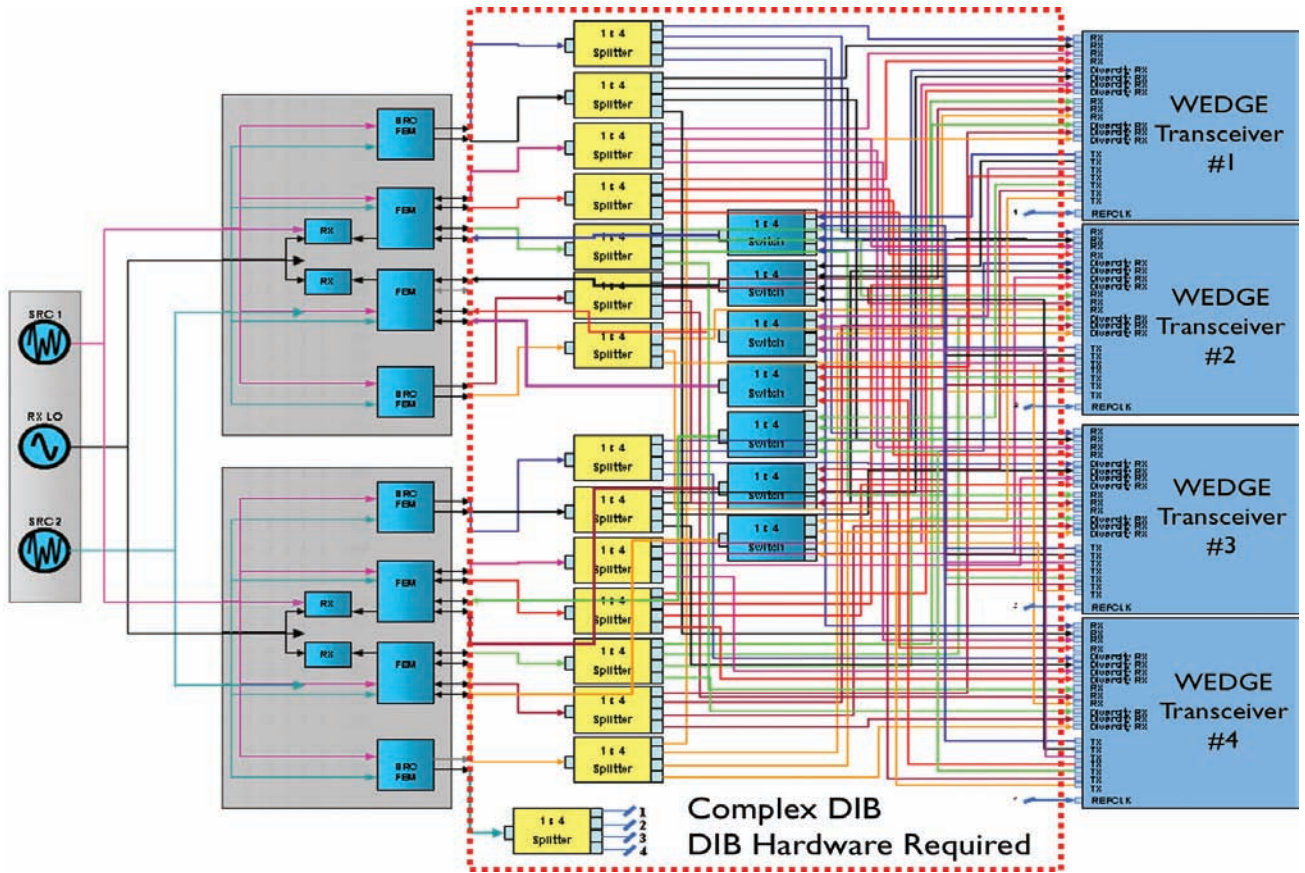


Figure 1. WEDGE Transceiver Quadsite 24-Port RF Solution

not all of the ports are identical. Some ports were designed to source only, others for receive, some for bidirectional operation. Some will have an excess noise ratio (ENR) source for noise figure (NF) testing, and some may have a low-noise amplifier (LNA) for low-power measurements.

With these nonuniversal ports, the 2G RF instrument configuration will limit certain connection possibilities. On an ATE system with 24 available ports, to design a quadsite DIB for a DUT with more than 12 RF ports will require that splitters, switching, and cabling hardware be added to the DIB to expand the ATE system’s resources. Introduction of this hardware will increase the effort required to complete the layout process of the DIB and inherently increase cost.

For the 22-port WEDGE device, configuring a DIB for the 24-port ATE system will require time to correctly map DUT pins to available system

resources. After the resource mapping has been completed, additional time will be required to choose the correct DIB hardware to expand the ATE instrument to all four sites.

One method to test the WEDGE receiver paths is to fan out an RF synthesizer to multiple RF pins in parallel by using a power splitter. For our example test case, a 1x4 power splitter could be used to fan out one synthesizer to test the primary receive paths for the quadsite solution. A second 1x4 splitter would be required to fan out a second synthesizer to diversity receive paths for the quadsite solution. As a result, 14 1x4 splitters would be needed to connect to the seven different pairs of primary/diversity receive pins for all four sites.

For WEDGE transmitter testing, fan-out connections to the ATE receiver instrument require a switch. For the WEDGE example, two 1x4 switches will fan out the ATE receiver

paths to cover all of the transmitter paths for a single device. Seven 1x4 switches would be required to fan out the ATE receiver ports to cover all of the device transmitter paths on the quadsite DIB.

Of the remaining two available ATE RF ports, one port provides a reference clock signal that must be split using a 1x4 power splitter to connect to all four sites in parallel. See **Figure 1**.

By now, the DIB layout for the required components to connect the RF has become very difficult: 15 1x4 power splitters, 48 controllable attenuators, 48 terminating switches, seven 1x4 switches, and 23 RF surface-mounted SMA, SMP, or similar connectors together with any additional baluns, attenuators, buffer circuits, and non-RF trace switches.

DIB Component Problems

A solution using DIB components to fan out RF signals has several problems:

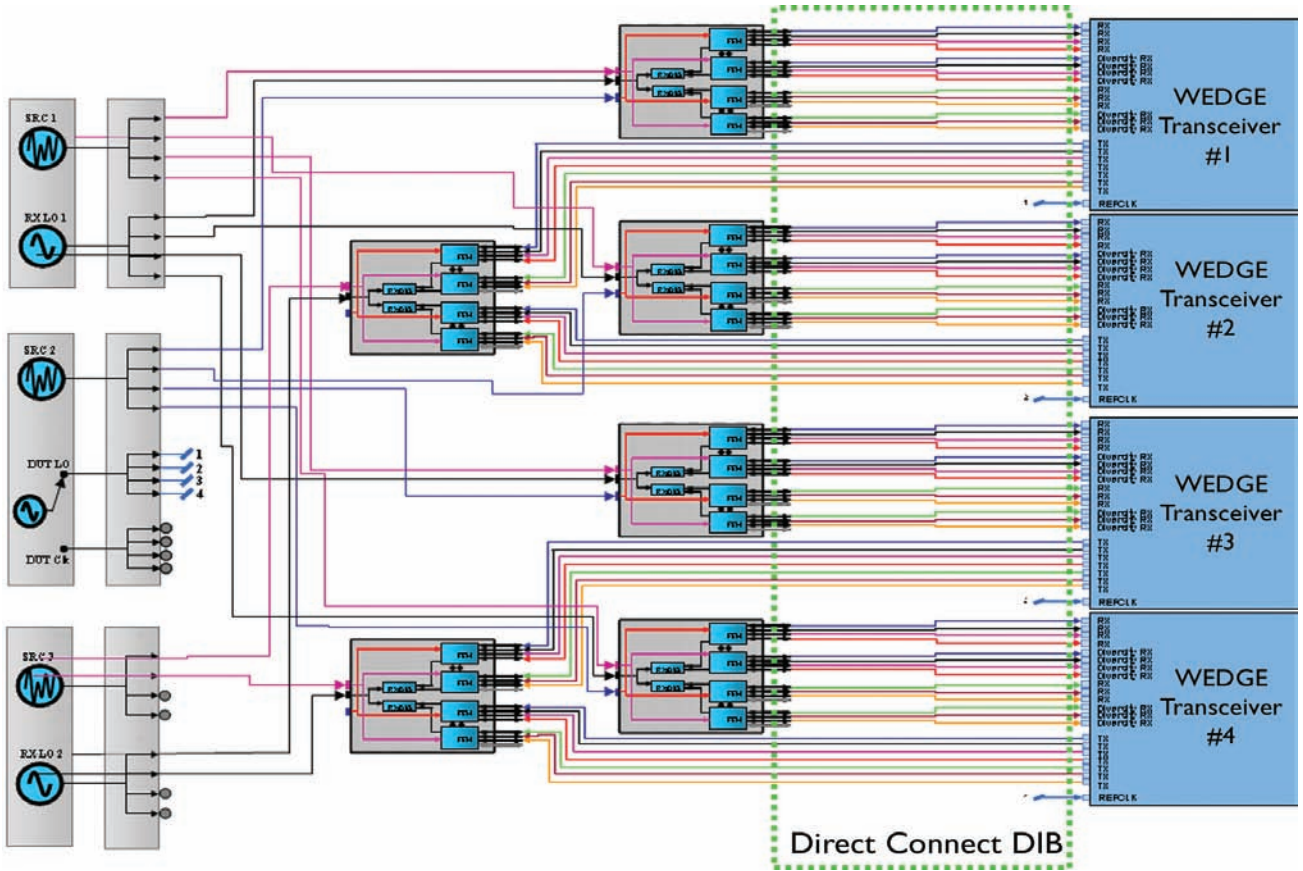


Figure 2. WEDGE Transceiver Quad-site 98-Port Direct-Connect RF Solution

- The introduction of DIB hardware into any RF system will directly reduce the main instrumentation’s accuracy and repeatability. This, in turn, will directly impact yield as guard bands are increased to account for additional losses.
- DIB power splitters cannot be perfectly balanced without the addition of controllable attenuation and a calibration routine that must be run at the start of the test. For any measurement associated with a connection path to an unbalanced DIB splitter, the results of a gage repeatability and reproducibility (GR&R) study will require tighter production guard bands that reduce yield and increase the COT.
- When sourcing through a DIB splitter to multiple sites, DIB circuitry should be used to manually manage connections to failed sites while protecting the remaining active sites from reflected signal power. So for a 1x4 splitter, each of the four output paths

must be connected to a controllable attenuator and then a switch before connection to the device.

- In the event that one or more sites have a gross failure, a 50-Ω termination to ground can be connected to protect the other sites. Besides the additional DIB hardware, the test engineer also must develop the software to manage the switches for this event, increasing the overall complexity of the project.
- Since the DIB will be mounted to a device handler, the majority of the components must be located on the tester side of the DIB or under a shield on the socket side to protect the components from the motion of the handler’s actuators.
- Using surface-mount components on the tester side of the DIB will require connection to the device using vias, which never are as good as a fully shielded connector to transition between layers. Each transition

produces a discontinuity and consequently an impedance mismatch adding series inductance.

- Additional DIB hardware will increase the time required to design the layout for the DIB as well as the time to develop the device test program.
- Every additional DIB-based RF interconnection also increases VSWR that makes channel matching more difficult.
- Each DIB will require more extensive engineering effort to characterize for release to production.
- More complex debug is required through the use of splitters/switches.

Next-generation RF ATE systems are designed for high port count devices and have universal bidirectional ports accessed by multiple virtual instruments. A better solution for these devices is to connect every RF pin directly to an available resource on the ATE system. This direct connection eliminates the need for any DIB-mounted splitters and switches.

To simplify DIB design problems, an ATE RF instrument with universal ports is essential. Universal RF ports reduce the time to complete layout since every port will be bidirectional and have the same capability and performance.

Using Universal Ports

A direct-connection approach using universal ports, as shown in **Figure 2**, has many benefits:

- DIB design has very low risk for RF test solutions. The RF layout designed for the first site is copied and pasted to create the layout for all remaining sites.
- The DIB is available several weeks faster due to shorter layout design times. This reduces the design/debug time cycle.
- All of the RF transmission lines remain on the top layer (handler side) of the DIB.
- Use fully shielded connectors to transition the RF signal paths through the DIB, removing the problem of using vias to transition between layers.
- Keep RF transmission lines short for improved matching capability.
- Lowering the DIB component count decreases hardware cost.
- A simplified DIB offers less worry in a production environment.
- With fewer components comes higher DIB reliability. Fewer DIBs will be required to support any overseas production.
- DIBs are easier to troubleshoot in production facilities.
- No custom RF DIB calibrations are required.

From start to finish, the complete DIB development cycle typically consumes several months of the project schedule. Using a direct-connect approach will reduce design risk, maintain the DIB development budget, and help to keep the project on track for a faster TTM release.

Test Program Development

The second challenge is test program development. With increased device integration, the production test program must control multiple instruments in parallel to power the device, load firmware, set the test mode, and

send/receive both digital data and RF signals.

The test engineer must develop the production test program for the best COT and parallel test efficiency. To achieve the highest parallel test efficiency, the majority of the program should be developed using pattern-oriented programming (POP). POP allows for setup and control of the ATE digital, analog, and RF instruments from the same pattern.

3G and 4G communications standards call for full duplex testing of the transceiver device, and POP will control ATE instrumentation for both transmit and receive in parallel for all sites. The typical test program for an RF SIP/SOC is very DSP intensive for both the transmit and receive portions of the device.

To minimize test time, DSP must be performed in parallel. The ATE system must have high-speed links between the DSP engines and both RF and digital instrumentation for full background processing.

The most difficult programming task for next-generation devices is the development of the modulated waveforms and demodulation DSP algorithms required to test the DUT. Until a few years ago, it was possible to test the typical transceiver using simple sine waves. Today, device integration and the rapid evolution of RF communications standards with increased bandwidths and more complex modulation requirements are driving test engineers to work closely with the ATE manufacturer in a constant effort to develop solutions.

To create a modulation/demodulation solution typically requires several months of work to read through the device standard to decipher the modulation requirements before coding can begin. To complete this task, it could take an additional five to nine months to develop reusable algorithms that cover all permutations of the standard.

For example, a modulated signal is created by building a mathematical I & Q segment that is frequency up-converted and sourced to a DUT. The development process can involve designing the header coding function,

data coding whether convolution encoder or other, interleaving function, and mapping function.

Similar to using a bench synthesizer, the creation of a modulated waveform should become a point-and-click operation to choose from a set of predefined waveforms for complex communications standards. This will reduce code development of the modulated waveform to minutes.

The demodulation algorithm will require building DSP functions to perform the bits comparator function, demapping function, deinterleaving function, data decoder whether viterbi decoder or other, header decoder function, and mapping function.

Once the signal has been demodulated and the data bits recovered, they must be processed further to get to a result. Code development continues with the creation of measurement functions to calculate error vector magnitude (EVM), phase error, bit error rate, time mask, spectral mask, adjacent channel leakage power ratio, and some simple spectrum analyzer-like functionality.

Correlating the test solution to the engineering bench requires that the ATE's demodulation algorithms provide direct one-to-one algorithmic correlation with the bench equipment used by engineering. Test engineers have a problem matching the results of ATE code to the results measured on a bench instrument with no capability to directly compare the algorithms.

When the code solution does not match the bench, the test engineer typically has no choice but to modify the program to achieve correlation. The test engineer may be lucky enough to call the bench instrument manufacturer's corporate support line and talk to an engineer who can help determine the major algorithm difference.

The desired solution would integrate the software from the bench equipment directly into the ATE's software solution (**Figure 3**). The correctly integrated solution results in the following:

- A cleanly integrated code/debug environment on the ATE system, with a simple code interface for the test engineer.

- A guaranteed one-to-one algorithmic correlation between the ATE solution and the engineering bench instrument.
- An optimized program execution on the ATE system, running fully in background on multiple DSP engines in parallel, which provides more than 95% parallel test efficiency.
- A reduced modulation/demodulation code development time compressing many months worth of coding effort into a matter of hours.
- A shortened amount of time required to correlate RF measurements between the ATE and bench instruments.

The correctly integrated solution also provides the power of the bench equipment's debug environment and real-time analysis. A test engineer should be able to stop at a trap in the program and open an integrated debug display to analyze the captured signal.

The GUI that opens must provide the capability to view the unprocessed time-domain capture, the RF spectrum, the constellation diagram, and results for EVM and phase error at the same time. Like the bench instrument, an active debug GUI that provides spectral analysis and demodulation capability will allow the test engineer to significantly shorten the development and debug time.

Conclusion

For 3/4G RF SIP/SOC devices, test engineers will greatly benefit from using a direct-connect universal port ATE RF system.

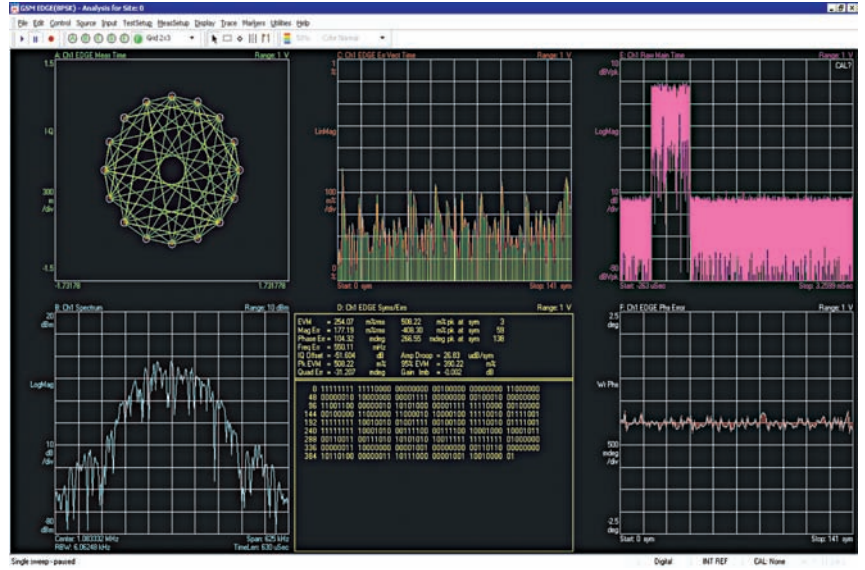


Figure 3. Vector Signal Analyzer Display from an Integrated-Solution

Test program development requires the next generation of ATE RF instrumentation. In today's consumer market place, ATE suppliers cannot afford to let increasing device complexity slow down TTM; they must provide the needed RF instrumentation and software tools today.

Moving the ATE system into the next generation of test will require an RF instrument with direct-connect universal ports and an integrated modulation/demodulation tool kit equivalent to bench instrumentation. This ATE system will shorten development time and allow the test engineer to optimize the production test solution for the best COT. Testing 3/4G devices becomes easier while allowing the test engineer to achieve both COT and TTM goals.

About the Author

Ron Burke is a senior RF applications engineer at Teradyne and a member of the company's RF instrumentation design team. His 11 years of RF/microwave ATE experience includes development of advanced test techniques implemented into production test solutions for RF transceiver devices. Mr. Burke received a B.S.E.E from the University of Massachusetts. Teradyne, Semiconductor Test Division, Factory Applications, 600 Riverpark Dr., North Reading, MA 01864, 978-370-2130, e-mail: ronald.burke@Teradyne.com

EE



600 Riverpark Drive, North Reading, MA 01864
978.370.2700 • www.teradyne.com